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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,429	07/10/2001	Qi Xiang	F0588	7718

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Mark D. Saralino
Renner, Otto, Boisselle & Sklar, LLP
1621 Euclid Avenue, 19th Floor
Cleveland, OH 44115

EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 12/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,429	XIANG ET AL.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 22-27* is/are pending in the application.

4a) Of the above claim(s) *15-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 22-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Paper No. 11, dated 10/14/03.

Drawings

New corrected drawings are required in this application because the figures are made by hand and are generally illegible. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14 and 22-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Thapar et al ('938).

In reference to claim 1, Thapar teaches a device comprising:

a) a central channel region comprising a first semiconductor lightly doped with a first impurity to increase first conductivity free carriers (Abs., lines: 1-15)

b) a source region and a drain region on opposing sides of the central channel region, both source and the drain regions being the first semiconductor heavily doped with the first impurity element (Abs.,lines: 1-15);

c) a gate adjacent the channel region and forming a junction with the channel region, the gate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers (Abs., lines: 1-25 and Col.6-7, lines: 65-8).

In reference to claim 2, Thapar teaches further including a backgate adjacent the channel region and on an opposing side of the channel region form the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carrier of the opposite conductivity as the first free carriers (Abs., lines: 1-25 and Col.6-7, lines: 65-8, see also Col.7, lines: 40-50).

In reference to claim 3, Thapar teaches wherein the first semiconductor is silicon (Abs.,lines: 15-25 and Col.3, lines: 25-35).

In reference to claim 4, Thapar teaches wherein the first conductivity free carriers are electrons and the second semiconductor is carbon and the first and second form a silicon carbide crystal structure (Col.4, lines: 55-65).

In reference to claim 5, Thapar teaches wherein the first conductivity free carriers are electrons and the second are holes (Col.3, lines: 55-68)

In reference to claim 6, Thapar teaches wherein the first impurity is As (Col.7, lines: 10-20)

In reference to claim 7, Thapar teaches wherein the second impurity is B (Col.4, lines: 10-15).

In reference to claim 8, Thapar teaches a device comprising:

a) an insulating oxide layer separating a device layer of semiconductor material from a bulk semiconductor base region (Col.3, lines: 1-10);

b) a generally rectangular central channel region within the device layer semiconductor material doped with a first impurity element to increase first conductivity free carriers (Col.5, lines: 60-68);

c) a source region and a drain region on opposing sides of the generally rectangular central channel region, both the source and drain comprising the device layer semiconductor material heavily doped with the first impurity element (Col.2, lines: 50-60)

d) a gate adjacent the channel region and extending along a side of the central channel region adjacent the source and forming a junction with the channel region, the gate comprising the device layer semiconductor and a second semiconductor with an energy gap greater than the device layer semiconductor and being doped with a second impurity element to increase carrier so the opposite conductivity as the first free carriers (Abs., lines: 1-25 and Col.6-7, lines: 65-8).

In reference to claim 9, Thapar teaches further including a backgate adjacent the channel region and on an opposing side of the channel region form the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carrier of the opposite conductivity as the first free carriers (Abs., lines: 1-25 and Col.6-7, lines: 65-8, see also Col.7, lines: 40-50).

In reference to claim 10, Thapar teaches wherein the first semiconductor is silicon (Abs.,lines: 15-25 and Col.3, lines: 25-35).

In reference to claim 11, Thapar teaches wherein the first conductivity free carriers are electrons and the second semiconductor is carbon and the first and second form a silicon carbide crystal structure (Col.4, lines: 55-65).

In reference to claim 12, Thapar teaches wherein the first conductivity free carriers are electrons and the second are holes (Col.3, lines: 55-68)

In reference to claim 13, Thapar teaches wherein the first impurity is As (Col.7, lines: 10-20)

In reference to claim 14, Thapar teaches wherein the second impurity is B (Col.4, lines: 10-15).

In reference to claim 22, Thapar teaches wherein the gate extends the entire length of the channel region between the source and drain ((Fig. 3D (128)).

In reference to claim 23, Thapar teaches further including a backgate adjacent the channel region and on an opposing side of the channel region form the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carrier of the opposite conductivity as the first free carriers (Abs., lines: 1-25 and Col.6-7, lines: 65-8, see also Col.7, lines: 40-50).

In reference to claim 24, Thapar teaches further including a conductive via electrically coupling the gate to the backgate (Col.5, lines: 25-35)

In reference to claim 25, Thapar teaches wherein the gate extends the entire length of the channel region between the source and drain ((Fig. 3D (128)).

In reference to claim 26, Thapar teaches further including a backgate adjacent the channel region and on an opposing side of the channel region form the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carrier of the opposite conductivity as the first free carriers (Abs., lines: 1-25 and Col.6-7, lines: 65-8, see also Col.7, lines: 40-50).

In reference to claim 27, Thapar teaches further including a conductive via electrically coupling the gate to the backgate (Col.5, lines: 25-35).

Response to Arguments

Applicant's arguments filed 10/14/03 have been fully considered but they are not persuasive. Applicant argues that the gate region does not consist of two different materials having two different energy gap dimensions, however this argument is not persuasive because as shown in Fig.3E and 3F of Thapar et al ('938), silicon carbide layer 116 is formed directly beneath gate 128 and therefore may be interpreted to be part of the gate region.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LMS

December 26, 2003

CARL WHITEHEAD JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800